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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,942	03/25/2004	Nicolas Carriere	02-GR1-123	6400

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EXAMINER	
GHYKA, ALEXANDER G	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,942	CARRIERE ET AL.	
	Examiner	Art Unit	
	Alexander G. Ghyka	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

ALEXANDER GHYKA
PRIMARY EXAMINER
AU 2812

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response of 5/1/2006 has been considered and entered. Claims 1 and 9 have been amended and Claims 4-5 and 15-16 have been cancelled. Claims 1-3 and 6-13 are pending. The Claim objections of the previous Office action are withdrawn in view of Applicants' amendments. The rejections under 35 USC 102 of the previous Office action are withdrawn in view of Applicants' amendments. With respect to the rejections under 35 USC 103, Applicants' arguments have been considered but they are not persuasive for the reasons as discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3 and 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al (US 6,271,133) in view of Tavel et al (Totally Silicided CoSi2 Polysilicon, IEEE pgs 37.5.1-4), "Tavel et al".

The present claims generally require a method for fabricating a transistor with a metal gate, that includes a siliciding phase comprising the formation, from a first metal, of a first metal silicide on the drain and source regions, while the gate region is protected by a layer of hard mask; removal of the hard mask; the formation, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal, wherein the first metal and the second metal are identical.

Lim et al disclose a transistor having silicided regions. Lim et al disclose protecting the gate region with a hardmask **20** (Figure 4), forming a layer of TiSi2 over the source/drain region by depositing a layer of titanium and annealing with the silicon substrate **31** (Figure 5), removing hardmask layer **20** (Figure 6), and the formation of, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal (Figures 7-8). See column 5, lines 30-45, column 6, lines 40-65 and column 7, lines 1-25. Lim et al disclose the annealing steps as required by present Claims 2, 8 and 10. See column 7, lines 15-25 and column 8, lines 25-35. Lim et al disclose that the first metal and the second metal comprise

cobalt or titanium. See column 4, lines 1-20. Moreover, Lim et al disclose that the hardmask is titanium nitride as required by present Claim 7. See column 4, lines 30-35.

Lim et al disclose the presently claimed limitations, with the exception of the formation of a cobalt silicide on both the source and drain and the gate regions, and completely siliciding the gate region.

Tavel et al disclose the formation of a completely silicided transistor which uses cobalt on the source, drain and gate regions and its benefit as a low gate resistivity transistors. See page 37.5.1 and Figure 1. Tavel et al disclose temperature ranges which are encompassed by the present Claims. See 37.5.2 second column, first paragraph. Tavel et al further disclose that extraordinarily low sheet resistance was measured on highly silicided structures. See page 37.5.2, second column, first full paragraph.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the same metal (cobalt) to silicide the silicided transistor of Lim et al, as disclosed by the Tavel et al reference, for its known benefit in forming a low gate resistivity transistor as disclosed by the Tavel reference. As the use of cobalt to silicide the source, drain and gate regions is known in the art as disclosed by Tavel, one of ordinary skill in the art would find it obvious to modify the Lim et al reference (which also discloses the use of cobalt) and use the same metal to silicide all three regions, for its known benefit in forming a silicided region transistor having low gate resistivity as disclosed by the Tavel et al reference. With respect to completely siliciding the gate

region, it would have been obvious for one of ordinary skill in the art to completely silicide the gate region in the process of Lim et al, for its known benefit of obtaining low sheet resistance as disclosed by the Tavel et al reference. With respect to the temperature ranges as required by the present claims, where the general conditions of a claim are disclosed in the prior art, in the present case both references disclose overlapping ranges, it is not inventive to discover the optimum or workable ranges by routine experimentation. See *Allen v.* Coe 57 USPQ 136. Therefore, a *prima facie* case of obviousness is established.

Claims 1-3 and 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sitaram et al (US 5,352,631) in view of Tavel et al (Totally Silicided CoSi2 Polysilicon, IEEE pgs 37.5.1-4), "Tavel et al".

The present claims generally require a method for fabricating a transistor with a metal gate, that includes a siliciding phase comprising the formation, from a first metal, of a first metal silicide on the drain and source regions, while the gate region is protected by a layer of hard mask; removal of the hard mask; the formation, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal, wherein the first metal and the second metal are identical.

Sitram et al disclose a transistor having silicided regions. Sitaram et al disclose protecting the gate region with a hardmask **20** (Figure 1), forming a layer of TiSi2 over the source/drain region by depositing a layer of titanium and annealing with the silicon substrate 12 (Figure 3), removing hardmask layer **20** (Figure 4), and the formation of, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal (Figures 5-8). See column 4, lines 15-60, and column 5, lines 1-55 . Sitaram et al disclose the annealing steps as required by present Claims 2, 8 and 10. See column 4, lines 25-40. Sitram et al disclose that the first metal and the second metal comprise cobalt or titanium. See column 4, lines 15-20 and column 5, lines 45-55.

Sitaram et al (US 5,352,631) et al disclose the presently claimed limitations, with the exception of the formation of a cobalt silicide on both the source and drain and the gate regions and completely siliciding the gate region.

Tavel et al disclose the formation of a silicided transistor which uses cobalt on the source, drain and gate regions and its benefit as a low gate resistivity transistors. See page 37.5.1 and Figure 1. Tavel et al disclose temperature ranges which are encompassed by the present Claims. See 37.5.2 second column, first paragraph. Tavel et al further disclose that extraordinarily low sheet resistance was measured on highly silicided structures. See page 37.5.2, second column, first full paragraph.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the same metal (cobalt) to silicide the silicided transistor of Sitaram et al , as disclosed by the Tavel et al reference, for its known benefit in forming a low gate resistivity transistor as disclosed by the Tavel reference. As the use of cobalt to silicide the source, drain and gate regions is known in the art as disclosed by Tavel, one of ordinary skill in the art would find it obvious to modify the Sitaram et al reference (which also discloses the use of cobalt) and use the same metal to silicide all three regions, for its known benefit in forming a silicided region transistor having low gate resistivity as disclosed by the Tavel et al reference. With respect to completely siliciding the gate region, it would have been obvious for one of ordinary skill in the art to completely silicide the gate region in the process of Sitram et al, for its known benefit of obtaining low sheet resistance as disclosed by the Tavel et al reference. With respect to the temperature ranges as required by the present claims, where the general conditions of a claim are disclosed in the prior art, in the present case both references disclose overlapping ranges, it is not inventive to discover the optimum or workable ranges by routine experimentation. See *Allen v.* Coe 57 USPQ 136. Therefore, a *prima facie* case of obviousness is established.

Response to Applicants' Arguments

Applicants argue that a person of ordinary skill in the art would not be inclined by Lim, Sitaram or any combination thereof to form a transistor having drain/source regions and gate with the same silicided metal, since both Lim and Sitaram

disclose a method for forming a transistor having drain/source regions and a gate in different silicided metals. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the present case the Tavel reference is used to show that having the drain/source and gate regions be of the same metal is known, as well as its benefit of low resistivity. Moreover, the Examiner notes that Sitaram does not require the metals to be different, and Lim notes that it is known to use the same metal in the background of the invention. See column 1, lines 30-45. Unpreferred embodiments must be considered in determining obviousness. See *In re Burckel*, 201 USPQ 67 (CCPA 1979). In the present case the use of different metals does not patentably differentiate from the cited prior art.

Applicants further argue that even if a person of ordinary skill in the art wanted to combine Lim and Tavel, or Sitaram and Tavel, the result would be a totally silicided gate transistor but with a different silicided method for source/drain regions and the gate. The Examiner maintains that in view of the cited prior art references, the use of the same metal is known. The use of different metals for the souce/drain and gate regions merely seems to be a preferred embodiment of the Sitram and Lim references. The Sitram and Lim references are used to show the use of a hardmask to form the different regions. The Examiner maintains that it would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the same metal (cobalt) to silicide the silicided

transistor of Sitaram et al or Lim et al, as disclosed by the Tavel et al reference, for its known benefit in forming a low gate resistivity transistor as disclosed by the Tavel reference. As the use of cobalt to silicide the source, drain and gate regions is known in the art as disclosed by Tavel, one of ordinary skill in the art would find it obvious to modify the Sitaram et al or Lim et al reference (which also discloses the use of cobalt) and use the same metal to silicide all three regions, for its known benefit in forming a silicided region transistor having low gate resistivity as disclosed by the Tavel et al reference. As all of the references are drawn to transistors having silicided regions, the use of the same metal in the source/drain and gate regions does not patentably distinguish the present Claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Friday during general business hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGG
July 6, 2006

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